

09/975,104

Snyder

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L# Hits Search String

Databases

L1	1	("5493723").PN.	USPAT
L2	6502	(ise or "in-system emulat\$6")	USPAT; EPO; JPO; DERWENT; IBM_TDB
L3	10	2 and (fpga or "field programmable")	USPAT; EPO; JPO; DERWENT; IBM_TDB
L4	0	in-system emulat\$6	USPAT; EPO; JPO; DERWENT; IBM_TDB
L5	2	in-system emulator or "in-system emulation"	USPAT; EPO; JPO; DERWENT; IBM_TDB
L6	25	emulat\$5 same (fpga and lock\$8)	USPAT; EPO; JPO; DERWENT; IBM_TDB
L7	294	emulat\$5 and ("device under test" or dut)	USPAT; EPO; JPO; DERWENT; IBM_TDB
L8	53	7 and lock\$8	USPAT; EPO; JPO; DERWENT; IBM_TDB
L9	10	5493723.uref.	USPAT; EPO; JPO; DERWENT; IBM_TDB

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Results of search set L3:

US 6754862 B1	Gaining access to internal nodes in a PLD	20040622	714/725
US 6754633 B1	Encoding a code signal into an audio or video signal	20040622	704/273
US 6704889 B2	Enhanced embedded logic analyzer	20040309	714/39
US 6536017 B1	System and method for translating a report file of one logic device to a constraints file of another logic device	20030318	716/3
US 6353921 B1	Hardware logic device emulating any of two or more FPGAs	20020305	716/17
US 6226779 B1	Programmable IC with gate array core and boundary scan capability	20010501	716/16
US 6134517 A	Method of implementing a boundary scan chain	20001017	703/28
US 6120551 A	Hardware logic device emulating an FPGA	20000919	716/17
US 6071314 A	Programmable I/O cell with dual boundary scan	20000606	716/17
US 5991908 A	Boundary scan chain with dedicated programmable routing	19991123	714/727

Results of search set L6:

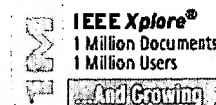
US 6732068 B2	Memory circuit for use in hardware emulation system	20040504	703/24
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US 6694464 B1	Method and apparatus for dynamically testing electrical interconnect	20040217	714/725
US 6691301 B2	System, method and article of manufacture for signal constructs in a programming		
US 6480954 B2	language capable of programming hardware architectures	20040210	717/114
US 6480952 B2	Method of time multiplexing a programmable logic device	20021112	713/1
US 6377912 B1	Emulation coprocessor	20021112	712/227
US 6263430 B1	Emulation system with time-multiplexed interconnect	20020423	703/28
US 6202044 B1	Method of time multiplexing a programmable logic device	20010717	713/1
US 6041428 A	Concurrent hardware-software co-simulation	20010313	703/28
US 5978260 A	Connection matrix for a microcontroller emulation chip	20000321	714/734
US 5960191 A	Method of time multiplexing a programmable logic device	19991102	365/182
	Emulation system with time-multiplexed interconnect	19990928	703/28
US 5959881 A	Programmable logic device including configuration data of user data memory	19990928	365/182
US 5943490 A	slices	19990824	703/28
	Distributed logic analyzer for use in a hardware logic emulation system		
US 5920712 A	Emulation system having multiple emulator clock cycles per emulated clock cycle	19990706	703/23
US 5838954 A	Computer-implemented method of optimizing a time multiplexed programmable		
	logic device	19981117	716/16
US 5825662 A	Computer-implemented method of optimizing a time multiplexed programmable		
	logic device	19981020	716/3
US 5784313 A	Programmable logic device including configuration data or user data memory	19980721	365/182
US 5778439 A	slices	19980707	711/153
US 5761483 A	Programmable logic device with hierarchical configuration and state storage	19980602	716/2
	Optimizing and operating a time multiplexed programmable logic device		
	Computer-implemented method of optimizing a design in a time multiplexed		
	programmable logic device	19971223	716/16
US 5701441 A	Time multiplexed programmable logic device	19970708	326/38
US 5646545 A	Method of time multiplexing a programmable logic device	19970513	326/93
US 5629637 A	Configuration modes for a time multiplexed programmable logic device	19970204	326/39
US 5600263 A	Sequencer for a time multiplexed programmable logic device	19961210	326/41
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1 Rapid prototyping of DSP systems: requirements and solutions

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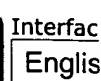
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